REMARKS

This application is a reissue application of U.S. Pat. No. 6,335,569. The application has been reviewed in light of the Office Action dated March 23, 2005.

Claims 1-37 are now presented for examination. Claims 1-21 and 35-37 have been allowed. Claims 22 and 29 have been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. Claims 22, 29 and 33 are independent. Favorable review is respectfully requested.

Claims 22-32 were rejected under 35 U.S.C. § 112, second paragraph, as failing to particularly point out and distinctly claim the subject matter of the invention. The Examiner stated that the term "sufficiently large" in independent claims 22 and 29 rendered the claims indefinite. Claims 22 and 29 have been amended to remove this phrase; the claims now recite that the upper surface is provided with a wear resistance in accordance with the size of the grains so as to prevent substantial scratching of the surface during polishing. See col. 3, lines 33-35; col. 5, lines 51-54; and col. 9, lines 53-55 of the '569 patent.

It is earnestly believed that all of the claims are now fully in compliance with 35 U.S.C. § 112. The Examiner is requested to contact the undersigned attorney if any further changes to the claims in this regard are necessary.

Claims 33 and 34 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nakasaki (U.S. Pat. No. 5,084,412). The applicant respectfully submits that independent claim 33 is patentably distinct from the cited art, for the following reasons.

The present invention, as defined in claim 33, is directed to a semiconductor structure which includes a plated soft metal layer interconnecting devices of a semiconductor chip. The soft metal is copper or alloy(s) thereof; the metal layer has a polished substantially scratch free surface.

It is thus a feature of the invention that (1) the metal layer is plated; and (2) the metal layer has a polished, substantially scratch free, surface.

Nakasaki is understood to disclose a copper wiring layer for a semiconductor device, in which a copper layer is deposited by sputtering (col. 8, line 3, and Fig. 2D), then patterned (Fig.

2E) and covered by a layer of chromium nitride (col. 8, lines 35-36, and Fig. 2F). According to Nakasaki, both the Cu layer and the underlying Cr layer are deposited by sputtering. Nakasaki does not disclose or suggest a plated metal layer as in the present invention, and in particular does not disclose or suggest a plated Cu or Cu-alloy metal layer. Furthermore, there is no suggestion in Nakasaki that the surface of the metal layer be polished. Indeed, Nakasaki makes no mention of any treatment of the surface of the copper layer, other than covering that surface with chromium nitride. In the method of Nakasaki, the process of covering the copper layer with chromium nitride is evidently performed without regard to the condition of the copper surface. It follows that Nakasaki neither discloses nor suggests that the copper layer have a substantially scratch free surface.

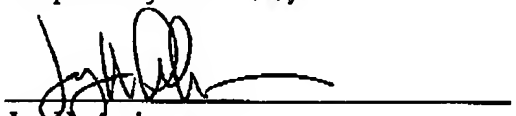
Since Nakasaki neither discloses nor suggests the above-noted features of the present invention, the present invention is not anticipated by that reference.

Claim 34, dependent from claim 33, includes all of the features of claim 33 and is therefore believed patentable for the same reasons as noted above.

In view of the foregoing amendments and remarks, the applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,



Jay H. Anderson
Attorney for Applicant
Registration No. 38,371

INTERNATIONAL BUSINESS MACHINES CORPORATION
Intellectual Property Law Department
B/321-482
2070 Route 52
Hopewell Junction, New York 12533
Facsimile: (845) 892-6363